WHAT IS CLAIMED IS:

1. A buffer circuit comprising:

a first transistor coupled between a first power source for supplying a first voltage of a first level and a first node, the first transistor having a gate for receiving a first signal having a first signal level;

a second transistor coupled between the first node and a second power source for supplying a second voltage of a second level, the second transistor having a gate for receiving a second signal having a second signal level, which is an inverse of the first signal level;

a third transistor having a gate coupled to the first node, the third transistor being coupled between the first power source and a second node;

a fourth transistor coupled between the second node and the second power source, the fourth transistor having a gate for receiving the first signal;

a fifth transistor having a gate coupled to the second node, the fifth transistor being coupled between the first power source and an output end; and

a sixth transistor having a gate coupled to the first node, the sixth transistor being coupled between the output end and the second power source, wherein capacitance is formed between the gate of the sixth transistor and the output end.

2. The buffer circuit of claim 1, further comprising an inverter for receiving the second signal and outputting the first signal, a third node for outputting the first signal being coupled to the gate of the first transistor.

3. The buffer circuit of claim 2, wherein the inverter comprises:

a seventh transistor coupled between the first power source and the third node, the seventh transistor having a gate for receiving the second signal; and

an eighth transistor being diode-connected, and being coupled between the third node and the second power source.

4. The buffer circuit of claim 2, wherein the inverter comprises:

a seventh transistor coupled between the first power source and the third node, the seventh transistor having a gate for receiving the second signal;

an eighth transistor coupled between the third node and the second power source, wherein another capacitance is formed between a gate of the eighth transistor and the third node; and

a ninth transistor being diode-connected, and being coupled between the gate of the eighth transistor and the second power source.

5. The buffer circuit of claim 1, further comprising a seventh transistor having a gate coupled to the output end, the seventh transistor being coupled between the gate of the fifth transistor and the second node.

6. The buffer circuit of claim 1, further comprising a seventh transistor having a gate coupled to the output end, the seventh transistor being coupled between the third and fourth transistors.

7. The buffer circuit of claim 1, further comprising:

a seventh transistor coupled between the first power source and the gate of the third transistor, the seventh transistor having a gate for receiving the first signal; and

an eighth transistor coupled between the gate of the third transistor and the second power source, the eighth transistor having a gate for receiving the second signal.

8. The buffer circuit of claim 1, further comprising:

a seventh transistor having a gate for receiving the second signal, the seventh transistor being coupled between the first power source and the gate of the first transistor; and

an eighth transistor having a gate for receiving the first signal, the eighth transistor being coupled between the gate of the first transistor and the second power source.

9. The buffer circuit of claim 1, wherein at least a part of the capacitance is formed by parasitic capacitance of the sixth transistor.

10. The buffer circuit of claim 1, wherein at least a part of the capacitance is formed by a capacitor coupled between the gate of the sixth transistor and the output end.

11. The buffer circuit of claim 1, wherein the first through sixth

transistors are PMOS transistors, the first level is a high level, and the second level is a low level.

12. The buffer circuit of claim 1, wherein the first through sixth transistors are NMOS transistors, the first level is a low level, and the second level is a high level.

13. A buffer circuit comprising:

a first transistor coupled between a first power source for supplying a first voltage of a first level and an output end;

a second transistor coupled between a second power source for supplying a second voltage of a second level and the output end, wherein capacitance is formed between the gate of the second transistor and the output end; and

a driving circuit for the first and second transistors, comprising a third transistor coupled between the gate of the second transistor and the second power source, the third transistor having a gate for receiving a first signal having a first signal level,

wherein the driving circuit turns on the first transistor and turns off the second transistor when the first signal level is substantially the first level, and

wherein the driving circuit turns on the third transistor to charge the capacitance with voltage, floats the gate node of the second transistor so that the second transistor can bootstrap, and turns off the first transistor, when the first signal level is substantially the second level.

14. The buffer circuit of claim 13, wherein the driving circuit further comprises:

a fourth transistor coupled between the first power source and the gate of the first transistor, the fourth transistor being turned on when the first signal level is substantially the second level; and

a fifth transistor coupled between the gate of the first transistor and the second power source, the fifth transistor being turned on when the first signal level is substantially the first level.

15. The buffer circuit of claim 14, wherein the driving circuit further comprises a sixth transistor having three terminals that are coupled, respectively, to the fourth transistor, the gate of the first transistor, and the output end.

16. The buffer circuit of claim 14, further comprising an inverter for receiving the first signal and outputting a second signal having a second signal level, which is an inverse of the first signal level, wherein a first node for outputting the second signal is coupled to the gate of the fifth transistor.

17. The buffer circuit of claim 14, comprising:

a sixth transistor coupled between the first power source and the gate of the fifth transistor, the sixth transistor having a gate for receiving the first signal; and

a seventh transistor coupled between the gate of the fifth transistor and the second power source, the seventh transistor having a gate for receiving a second signal having a second signal level, which is an inverse of the first signal level.

18. An active matrix display comprising:

a plurality of buffer circuits, each of the plurality of buffer circuits comprising:

a first transistor coupled between a first power source for supplying a first voltage of a first level and a first node, the first transistor having a gate for receiving a first signal having a first signal level;

a second transistor coupled between the first node and a second power source for supplying a second voltage of a second level, , the second transistor having a gate for receiving a second signal having a second signal level, which is an inverse of the first signal level;

a third transistor having a gate coupled to the first node, the third transistor being coupled between the first power source and a second node;

a fourth transistor coupled between the second node and the second power source, the fourth transistor having a gate for receiving the first signal;

a fifth transistor having a gate coupled to the second node, the fifth transistor being coupled between the first power source and an output end; and

a sixth transistor having a gate coupled to the first node, the sixth transistor being coupled between the output end and the second power source, wherein capacitance is formed between the gate of the sixth transistor and the output end;

a driving signal supply for supplying a plurality of first driving signals as the second signals to the plurality of buffer circuits, respectively; and

a display panel including: a plurality of first signal lines for transmitting the first driving signals that are passed and output, respectively, through the buffer circuits; a plurality of second signal lines for respectively transmitting a plurality of second driving signals, the second signal lines being formed crossing the first signal lines; and pixel circuits coupled to the first and second signal lines, the pixel circuits being operable by the first and second driving signals.

19. An active matrix display comprising:

a plurality of buffer circuits, each of the plurality of buffer circuits comprising:

a first transistor coupled between a first power source for supplying a first voltage of a first level and an output end;

a second transistor coupled between a second power source for supplying a second voltage of a second level and the output end, wherein capacitance is formed between the gate of the second transistor and the output end; and

a driving circuit for the first and second transistors, comprising a

third transistor coupled between the gate of the second transistor and the second power source, the third transistor having a gate for receiving a first signal having a first signal level,

wherein the driving circuit turns on the first transistor and turns off the second transistor when the first signal level is substantially the first level, and

wherein the driving circuit turns on the third transistor to charge the capacitance with voltage, floats the gate node of the second transistor so that the second transistor can bootstrap, and turns off the first transistor, when the first signal level is substantially the second level;

a driving signal supply for supplying a plurality of first driving signals as the first signals to the plurality of buffer circuits, respectively; and

a display panel including: a plurality of first signal lines for transmitting the first driving signals that are passed and output, respectively, through the buffer circuits; a plurality of second signal lines for respectively transmitting a plurality of second driving signals, the second signal lines being formed crossing the first signal lines; and pixel circuits coupled to the first and second signal lines, the pixel circuits being operable by the first and second driving signals.

20. A bootstrap circuit comprising:

a first transistor coupled between a first power source for supplying a first voltage of a first level and an output end;

a second transistor coupled between the output end and a second

power source for supplying a second voltage of a second level, , wherein capacitance is formed between a gate of the second transistor and the output end; and

a driving circuit for receiving first and second signals having first and second signal levels, respectively, that are inverse of one another, and respectively turning on the first transistor and turning off the second transistor when the first signal level is substantially the first level, wherein

the driver circuit applies a third voltage which has substantially the same voltage level as the second level to the gate of the second transistor to charge the capacitance with voltage, floats the gate node of the second transistor, and turns off the first transistor to bootstrap the second transistor, when the first signal level is changed to substantially the second level from substantially the first level.